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EXAMINER	
FIEGLE, RYAN PAUL	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,678	JACOB ET AL.	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 20-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 20-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 14-18 and 20-22 are objected to because of the following informalities:

The article "a" should be omitted from the end of line 2 of claim 14 since the receiving noun is now plural. Appropriate correction is required.

Claim 20 is still dependent on claim 19, which has been cancelled by the applicant. For the purposes of this action, claim 20 is now dependent on claim 19's parent, claim 18.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 7-9, 14, 16, 17, 22, 23 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Master et al. (US PGPub 2002/0138716).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in

the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

4. As per claim 1:

Master et al. teach an integrated circuit comprising:

a plurality of computational (¶45);

a first and a second processing node each having a core processor with a common architecture (¶12; ¶47; ¶28) (Paragraph 12 shows that they have common architectures. Paragraph 47 shows that each matrix has a core. Paragraph 28 that either the KARC or MARC can constitute a first node.), wherein the common architecture is configurable in response to a first configuration command to be a control node adapted to control an interconnection of said computational elements to perform a selected task and configure in response to a second configuration command to be a programmable scalar node (PSN) adapted to perform a computational application (¶29);

a first memory associated with said first processing node; a second memory associated with said second processing node (¶44; Figure 4) (Paragraph 44 shows that each mode has local memory. Figure 4 shows that the memory is associated with the core of the node.);

a first interface for coupling said core processor of said first processing node to said first memory and to said computational elements (¶29; ¶45; ¶47; Figure 3, data interconnect network);

a second interface for coupling said core processor of said second processing node to said second memory and to said computational elements, the first interface and

the second interface having the same architecture (¶25; ¶29; ¶45; ¶47) (Paragraph 25 shows that the MARC and KARC are made of the same matrices as the first processing node, and therefore will be set up the same way.).

5. As per claim 2:

The integrated circuit of claim 1 further comprising means for temporally adapting said second node and said computational elements to perform a selected function (¶40).

6. As per claim 3:

The integrated circuit of claim 2 wherein said temporal means further comprises executable code defining said selected function stored in at least a memory (¶40).

7. As per claim 7:

The integrated circuit of claim 1 wherein said computational elements include a plurality of arithmetic nodes, a plurality of bit-manipulation nodes and a plurality of finite state machine nodes (¶45).

8. As per claim 8:

The integrated circuit of claim 1 further comprising a plurality of said second processing nodes and an interconnection network, the plurality of said second processing nodes coupled through the interconnection network to said first processing node and plurality of computational elements (¶26; Figure 1).

9. As per claim 9:

An integrated circuit comprising:

a first node having:

a first core processor configurable in response to a first configuration signal into a controller node for execution of operating system code (¶26, ¶29);

a first memory for storing operating system executable code (¶44);

means for transferring operating system executable code and data from said first memory to said first core processor (¶29);

a plurality of computational elements adapted to perform a selected function (¶33)

a second node having:

a second core processor having the same circuit architecture as the first core processor, the second core processor configurable into a RISC processor for execution of application code (¶28);

a second memory for storing application code (¶44);

means for transferring application code and data from said second memory to said second core processor (¶29); and

an interconnection network coupling said controller node and said RISC processor to said plurality of computational elements to perform the selected function (¶26) (Figure 1, item 110);

a first interface coupling said first core processor to said interconnection network (Figure 1, item 110) (Part of matrix interconnection network 110 connects the individual matrices into the network); and

a second interface coupling said second core processor to said interconnection network, the first and second interfaces having a common interface architecture (Figure

1, item 110) (Part of matrix interconnection network 110 connects the individual matrices into the network).

10. As per claim 14:

An integrated circuit having a plurality of computational elements and an interconnection network for interconnecting said computational elements, said integrated circuit comprising:

a controller node comprising:

a first core processor for executing operating system code (¶47);

a first memory for storing operating system executable code (¶44); and

a first interface coupled to said first core processor and to the interconnect network, for receiving and transferring to the first core processor a portion of an input stream from an external source, said input stream having configuration information or executable code (¶29); and

a programmable scalar node comprising:

a second core processor for executing instructions, the second core processor having the same circuit architecture as the first core processor (¶28, ¶29);

an instruction memory for storing said instructions (¶44);

a data memory (¶44);

a second interface coupled to said second core processor and to the interconnection network for receiving an input stream from the controller node, said input stream having configuration information (¶29).

11. As per claim 16:

The integrated circuit of claim 14 further comprising means for node-to-node communication (¶29).

12. As per claim 17:

The integrated circuit of claim 14 further comprising a second memory for storing executable code for controlling the interconnection of said computation elements in response to configuration information (¶40).

13. As per claim 22:

The integrated circuit of claim 14 further comprising means for controlling power consumption (Abstract).

14. As per claim 23:

The integrated circuit of claim 1, wherein the control node is configured to change the interconnecting of said computational elements and said first and second processing nodes to define a second task to achieve a second function previously not available or existent (¶41).

15. As per claim 25:

The integrated circuit of claim 9, wherein the controller node is configured to change the interconnection network coupling said controller node to said computational elements to perform a second selected function not available or existent (¶41).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 4-6 and 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Master et al. (US Patent 2002/0138716) as applied to claims 3 and 17 above in view of Fallside et al. (US Patent 6,326,806).

18. Master et al. teach claims 3 and 17 for the reasons stated above.

19. As per claim 4:

Master et al. does not teach the integrated circuit of claim 3 wherein said executable code is downloaded from the Internet by said first processing node in which Fallside et al. do (Fallside et al.: column 1, lines 63-67; column 2, lines 1-9).

Fallside et al. comment that FPGA systems are at a disadvantage because reconfiguring an FPGA requires special hardware, while other systems can be upgraded from the Internet. Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Fallside et al. to Master et al. would provide the advantage of easier reconfiguration by using the Internet.

20. As per claim 5:

The integrated circuit of claim 4 wherein said executable code comprises operating system code (Master et al.: ¶41).

21. As per claim 6:

The integrated circuit of claim 5 wherein said first processing node initiates the temporal adaptation of said computational elements and said second processing node to perform said selected function (Master et al.: ¶41).

22. As per claim 18:

The integrated circuit of claim 17 further comprising means for controlling an initiation of operation of said computational element upon reset or power on (Fallside et al.: column 2, lines 2-9) (Motivation for applying Fallside to Master is provided above).

23. As per claim 20:

The integrated circuit of claim 18 further comprising:

a data cache; and

an instruction cache (Official Notice) (Though Masters does not disclose an instruction cache and a data cache, such are very well known in the art as well as their known advantages, and it is obvious to see why Master et al. would have motivation to add them).

24. As per claim 21:

The integrated circuit of claim 20 further comprising a memory arbitration unit for managing access to said data memory and said instruction memory (Master et al.: ¶29) (The interconnection network takes care of memory accesses).

25. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Master et al. (US Patent 2002/0138716) as applied to claim 9 above in view of Trimberger et al. (US Patent 5,646,545).

26. Master et al. teach claim 9 for the reasons stated above.

27. As per claim 10:

Master et al. do not teach the integrated circuit of claim 9 wherein said first node further comprises a configuration register, said configuration register containing a bit for determining whether said first node functions as the controller node or as a RISC processor.

Though Master states that the controller can be a FSM or a RISC processor, he does not disclose changing between these two configurations.

Trimberger discloses a state register, which keeps track which configuration a FPGA is in and blocks other memory cells containing other configurations while in that state (Trimberger et al.: Abstract).

Trimberger states that prior ways of reconfiguring FPGAs is time consuming and that his method will save time in reconfiguring (Trimberger et al.: column 1, lines 50-61).

Therefore, it would have been obvious to one of ordinary skill in the pertinent art at the time of the applicant's invention that applying Trimberger et al. to Master et al. would make the reconfiguration of the controller faster.

28. As per claim 11:

The integrated circuit of claim 10 wherein said configuration register bit, when set, protects a portion of memory from access by said computational elements (Trimberger et al.: Abstract).

29. As per claim 12:

The integrated circuit of claim 10 further comprising a protected portion of memory accessible only to said controller node (Master et al.: ¶44).

30. As per claim 13:

The integrated circuit of claim 9 wherein said first node and said second node further comprise:

an interface having:

a data distributor for receiving an input stream from an external source, said input stream having configuration information, application code, or executable code (Master et al.: ¶29, ¶40, ¶41);

a hardware task manager for receiving configuration information from said data distributor (Master et al.: ¶41);

a DMA engine for receiving data and executable code from said data distributor (Master et al.: ¶29; ¶40);

a controller for providing said interface access to a set of registers associated with the corresponding first or second core processor (Master et al.: ¶47); and

an interrupt controller for detecting an interrupt condition (Master et al.: ¶29) (The network interconnect handles control and I/O signals which cause interrupts; an interrupt controller is inherent since the interrupts need to be handled.

31. Claims 15 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Master et al. (US Patent 2002/0138716) as applied to claims 14 and 9 above, respectively.

32. Master et al. teach claim 14 for the reasons stated above.

33. As per claim 15:

Master et al. do not teach the integrated circuit of claim 14 further comprising means for accessing said first core processor and said first memory to debug error conditions.

This would entail a JTAG controller, which is well known in the art along with its many known advantages, and it is obvious to see why Master et al. would have motivation to add it (Official Notice).

34. As per claim 25:

While Master does not explicitly state that the PSN nodes (Figure 1, items 150E-N) can be configured as RISC processors, such would have been inherent since the logic required to implement a RISC processor is present in the nodes (¶28) and RISC processors are well known to be able to perform various tasks which would be beneficial to Mater's system.

Response to Arguments

35. The applicant has made the following argument:

> "First Master does not disclose or suggest a *common* core architecture that is *configurable* (in different, first and second nodes) to be a control node for controlling the interconnecting of the computational elements and also configurable to be a programmable scalar node (PSN) for performance computational applications. Second, Master does not disclose and does not suggest that such a core processor would be coupled to a defined, *uniform interface*, referred to in the specification as a 'node wrapper', which provides a uniform communication interface to and from all nodes, including the control node and the PSN. Third, Master fails to disclose or suggest that the first processing node is configured as the control node based on a first configuration command, and the second processing node is configured as the PSN node based on a second configuration command." (citation omitted)

Master *does* teach a common core architecture that is configurable (¶12).

Master *does* teach a uniform interface to provide uniform communication interface to and from all nodes, including the control node and the PSN (¶26).

Master *does* teach that the first processing node is configured as the control node based on a first configuration command and the second processing node is configured as the PSN node based on a second configuration command (¶29) (configuration information).

36. The applicant has made the following argument:

> "However, Master does not disclose or suggest that controller 120 includes the same core processor based on a common architecture as computational units 200."

The applicant has misread Master. Computational units 200 are a ***part*** of controller 120, not a "second processing node" (¶31; Figure 1; Figure 3). Specifically, controller 120 is made up of matrices 150, which are made up of computational units 200, which are made up of computational elements 250. All other matrices 150 are used for functionality and memory (¶25). Each matrix 150 contains multiple computational units 200, which all contain a common core 260 based on the ACE architecture which is used to configure and reconfigure all of the matrices for particular functionalities (¶12).

37. The applicant has made the following argument:

> "In addition there is no motivation to combine these references [of Master, Fallside and Trimberger."

Motivation for combining Master and Fallside is clearly provided in section 16 of the previous office action. Motivation for combining Master and Trimberger has been shown in section 25 of the previous office action.

Conclusion

38. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan P Fiegle
Examiner
Art Unit 2183

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